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## **CLAIMS**

What is claimed is:

1. A semiconductor chip having low metallization series resistance, comprising:

a semiconductor substrate;

a metallization structure formed on said semiconductor substrate;

a UBM layer formed over said metallization structure;

a conductive bump formed over said UBM layer;

wherein the largest linear dimension of said UBM layer is larger than the diameter of said conductive bump.

- The semiconductor device as in claim 1 wherein said metallization structure further comprises a top metallization layer having said UBM layer formed thereover, wherein the thickness of said top metallization layer is substantially smaller than said UBM layer.
- 3. The semiconductor device as in claim 2 wherein said top metallization layer includes aluminum.
  - 4. The semiconductor device as in claim 1 wherein said UBM layer comprises a bottom layer of a metal that adheres to said metallization structure, a middle layer of a barrier metal, and a top layer of a conductive solderable metal.
- 5. The semiconductor device as in claim 4 wherein said bottom layer includes aluminum, titanium, or chromium.

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6. The semiconductor device as in claim 4 wherein said middle layer includes nickel.

- 7. The semiconductor device as in claim 4 wherein said middle layer includes vanadium.
- 5 8. The semiconductor device as in claim 4 wherein said top layer includes copper.
  - 9. The semiconductor device as in claim 4 wherein said top layer includes gold.
  - 10. A semiconductor chip having low metallization series resistance, comprising: a semiconductor substrate;
    - a top metallization layer formed on said semiconductor substrate;
- a UBM layer formed over said top metallization layer; wherein the thickness of said top metallization layer is substantially smaller than said UBM layer.
  - a conductive bump formed over said UBM layer;
  - wherein the largest linear dimension of said UBM layer is larger than the diameter of said conductive bump.
- 15 11. The semiconductor substrate as in claim 10 wherein said top metallization layer includes aluminum.
  - 12. The semiconductor device as in claim 10 wherein said top metallization layer includes aluminum.

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13. The semiconductor device as in claim 10 wherein said UBM layer comprises a bottom layer of a metal that adheres to said metallization structure, a middle layer of a barrier metal, and a top layer of a conductive solderable metal.

14. The semiconductor device as in claim 13 wherein said bottom layer includes aluminum, titanium, or chromium.

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- 15. The semiconductor device as in claim 13 wherein said middle layer includes nickel.
- 16. The semiconductor device as in claim 13 wherein said middle layer includes vanadium.
- 10 17. The semiconductor device as in claim 13 wherein said top layer includes copper.
  - 18. The semiconductor device as in claim 13 wherein said top layer includes gold.